CLAIMS

What is claimed is:

1. A magnetic memory element, comprising a plurality of stacked, closed-ended layers defining an opening therethrough, wherein the plurality of layers includes:

a reference magnetic layer having a permanent magnetic helicity;

a storage magnetic layer having two conjugate segments with opposing magnetic helicities; and

a non-magnetic layer between the reference layer and the storage layer.

2. The memory element of claim 1, wherein the aperture is offset from a center of the stacked layers.

3. The memory element of claim 1, wherein the plurality of closed-ended layers includes a plurality of annular layers.

4. The memory element of claim 1, wherein the non-magnetic layer includes an electrically conductive material.

5. The memory element of claim 4, wherein the non-magnetic layer includes Cu.

6. The memory element of claim 1, wherein the non-magnetic layer includes a non-electrically conductive material.

7. The memory element of claim 6, wherein the non-magnetic layer includes Al_2O_3.

8. The memory element of claim 1, wherein the reference layer, the storage layer and the non-magnetic layer constitute a magnetic tunnel junction structure.

9. The memory element of claim 1, wherein the reference layer, the storage layer and the non-magnetic layer constitute a first GMR structure.

10. The memory element of claim 9, further comprising a second GMR structure.

11. The memory element of claim 1, wherein the storage layer includes at least one nodule.

12. A memory cell, comprising:

a magnetic memory element including a plurality of stacked, closed-ended layers defining an opening therethrough, wherein the plurality of layers includes:

a reference magnetic layer having a permanent magnetic helicity;

a storage magnetic layer having two conjugate segments with opposing magnetic helicities; and

a non-magnetic layer between the reference layer and the storage layer;

an electrically conductive set line disposed through the opening of the magnetic memory element; and

a single transistor connected to the set line.

13. The memory cell of claim 12, wherein the aperture of the magnetic memory element is offset from a center of the magnetic memory element.

14. The memory cell of claim 12, wherein the transistor is for controlling access to the magnetic memory element for read and write operations.

15. The memory cell of claim 14, wherein the reference layer, the storage layer and the non-magnetic layer of the magnetic memory element constitute a magnetic tunnel junction structure.

16. The memory cell of claim 14, wherein the reference layer, the storage layer and the non-magnetic layer of the magnetic memory element constitute a GMR structure.

17. A memory device, comprising a plurality of magnetic memory elements, each magnetic memory element including a plurality of stacked, closed-ended layers defining an opening therethrough, wherein the plurality of layers includes:

a reference magnetic layer having a permanent magnetic helicity;

a storage magnetic layer having two conjugate segments with opposing magnetic helicities; and

a non-magnetic layer between the reference layer and the storage layer.

18. The memory device of claim 17, wherein the magnetic memory elements are arranged in a 2D array.

19. The memory device of claim 18, wherein the reference layer, the storage layer and the non-magnetic layer of the magnetic memory element constitute a magnetic tunnel junction structure.

20. The memory device of claim 18, wherein the reference layer, the storage layer and the non-magnetic layer of the magnetic memory element constitute a GMR structure.

21. The memory device of claim 17, wherein the aperture of at least one of the magnetic memory elements is offset from a center of the magnetic memory element.

22. A memory device, comprising:

a plurality of memory cells, each memory cell including:

a magnetic memory element including a plurality of stacked, closed-ended layers defining an opening therethrough, wherein the plurality of layers includes:

a reference magnetic layer having a permanent magnetic helicity;

a storage magnetic layer having two conjugate segments with opposing magnetic helicities; and

a non-magnetic layer between the reference layer and the storage layer;

an electrically conductive set line disposed through the opening of the magnetic memory element; and

a single transistor connected to the set line; and

at least one addressing circuit connected to the plurality of memory cells.

23. The memory device of claim 22, wherein the transistor of each of the memory cells is for controlling access to the magnetic memory element of the respective memory cell for read and write operations.

24. The memory device of claim 22, wherein the reference layer, the storage layer and the non-magnetic layer of the magnetic memory element constitute a magnetic tunnel junction structure.

25. The memory device of claim 22, wherein the reference layer, the storage layer and the non-magnetic layer of the magnetic memory element constitute a GMR structure.

26. The memory device of claim 22, wherein the magnetic memory elements are arranged in a 2D array comprising a plurality of columns and rows.

27. The memory device of claim 26, wherein a control terminal of the transistor of each memory in a column of the array is coupled to a bit line.

28. The memory device of claim 27, wherein the at least one addressing circuit includes one addressing circuit connected to each row of memory cells in the array.

29. The memory device of claim 22, wherein the aperture of at least one of the magnetic memory elements is offset from a center of the magnetic memory element.

30. A computing device, comprising:

a processor; and

a memory device in communication with the processor, wherein the memory device includes a plurality of magnetic memory elements, each magnetic memory element including a plurality of stacked, closed-ended layers defining an opening therethrough, wherein the plurality of layers includes:

a reference magnetic layer having a permanent magnetic helicity;

a storage magnetic layer having two conjugate segments with opposing magnetic helicities; and

a non-magnetic layer between the reference layer and the storage layer.

31. The computing device of claim 30, wherein the reference layer, the storage layer and the non-magnetic layer of the magnetic memory element constitute a magnetic tunnel junction structure.

32. The computing device of claim 30, wherein the reference layer, the storage layer and the non-magnetic layer of the magnetic memory element constitute a GMR structure.

33. The computer device of claim 30, wherein the aperture of at least one of the magnetic memory elements is offset from a center of the magnetic memory element.